In the Figures:

Please change FIGS. 1-4 as indicated in red on the attached copies.

In the Claims:

Please amend Claims 1, 7 and 12 as follows:

1. (Amended) A flip-flop circuit for reducing the current spike, comprising:

an input for receiving first data and second data, said first data being received and stored within said flip-flop circuit prior to said input receiving said second data, said first data being isolated from said second data, said input being controlled by a first clock signal; and

an output for transmitting said [second] first data [received by] after said input receives [prior to] said [first] second data, said output being controlled by a second clock signal, said first and second clock signals having the same frequency and substantially the same phase, wherein the arrival times of said first and second clock signals at said flip-flop are [at least slightly] skewed.

7. (Amended) A sequential logic circuit, comprising:

a first flip-flop having an input for receiving data and an output for transmitting said data, at least said output of said first flip-flop being controlled by a first clock signal;

combinational logic connected to said first flip-flop for receiving said data from said first flip-flop; and

a second flip-flop connected to said combinational logic having an input for receiving said data from said combinational logic and an output for transmitting said data, said input of said second flip-flop being controlled by said first clock signal, said output of said second flip-flop being controlled by a second clock signal, said first and second clock signals having the same frequency and substantially the same phase, wherein the arrival times of said first and second clock signals at said second flip-flop are [at least slightly] skewed.

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12. (Amended) A method for reducing current spikes within a logic circuit, comprising the steps of:

receiving data by a first flip-flop;

transmitting said data to combinational logic connected to said first flip-flop, said step of transmitting being controlled by a first clock signal;

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